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(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device which is easy to mount and improves the packing density.
SOLUTION: A first bare chip 1 has an element-forming face on which corresponding pads are formed to pads formed on an element-forming face of a second bare chip 2 flip-chip-mounted on the element-forming face of the first bare chip 1 with the chip 2 element-forming face down. On the periphery of the first chip 1 external connecting pads 5 are formed, corresponding to the input/output terminals of the first and second chips 1, 2, and connected to pads 8 on a printed wiring board 6 through bonding wires 9. The external connection pads are formed only on the bare chip 1 at the lower stage, thus facilitating the wire bonding work for the COB(chip-on-board)

mounting.

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CLAIMS

[Claim(s)]
[Claim 1] It has the 1st bare chip cut down from the semi-conductor wafer, and the 2nd bare chip which is cut down from a semi-conductor wafer and mounted in the top-face side of said 1st bare chip. Two or more pads are formed in the location which counters the top face of said 1st bare chip, and the inferior surface of tongue of said 2nd bare chip, respectively. The pad which counters is connected through a bump, respectively. In the top face of said 1st bare chip It is the semiconductor device which the pad for external connection corresponding to a part of input/output terminal [at least] of said 1st and 2nd bare chips is formed, and is characterized by connecting the pad for these external connection with the pad on a substrate through a bonding wire.
[Claim 2] In claim 1 said 1st bare chip It has the 1st pad train formed in that top face,

and the 2nd pad train formed in the periphery side rather than this 1st pad train. Used in order that said 1st pad train may carry out flip chip mounting of said 2nd bare chip, said 2nd pad train is COB (Chip On Board) to a printed wired board about said 1st bare chip. Semiconductor device characterized by being used since it mounts.

[Claim 3] The semiconductor device characterized by having the bare chip cut down from the semi-conductor wafer, forming in the inferior surface of tongue of said bare chip the pad on a substrate, and two or more pads connected through a bump, and forming in the top face of said bare chip the pad on a substrate, and two or more pads connected through a bonding wire.

[Claim 4] It has the 1st bare chip cut down from the semi-conductor wafer, and the 2nd bare chip which is cut down from a semi-conductor wafer and mounted in the inferior-surface-of-tongue side of said 1st bare chip. The semiconductor device characterized by forming in the inferior surface of tongue of said 2nd bare chip the pad on a substrate, and two or more pads connected through a bump, and forming in the top face of said 1st bare chip the pad on a substrate, and two or more pads connected through a bonding wire.

[Claim 5] It is the semiconductor device which two or more pads are formed in the location which counters the inferior surface of tongue of said 1st bare chip, and the top face of said 2nd bare chip, respectively in claim 4, and is characterized by connecting these pads through a bump.

[Claim 6] It has the 1st bare chip cut down from the semi-conductor wafer, and the 2nd bare chip which is cut down from a semi-conductor wafer and mounted in the inferior surface of tongue of said 1st bare chip. The pad on a substrate and two or more pads connected through a bonding wire are formed in the top face of said 1st bare chip. It is the semiconductor device which two or more pads are formed in the location which counters the inferior surface of tongue of said 1st bare chip, and the top face of said 2nd bare chip, respectively, and is characterized by connecting these pads through a bump.

[Claim 7] It is the semiconductor device which said 2nd bare chip is a memory chip or a CPU circumference chip, and is characterized by said 1st bare chip being a CPU chip in either of claims 1, 2, 4-6.

[Claim 8] It is the semiconductor device characterized by said each of 1st and 2nd bare chips being memory chips in either of claims 1, 2, 4-6.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the semiconductor device mounted in various substrates, such as a printed wired board.

[0002]

[Description of the Prior Art] It was tended to enlarge a computer program, and if the memory of sufficient amount for a computer machine is not carried, also when not operating to satisfaction, it has increased. For this reason, the usual computer machine has structure which can perform an addition and exchange of SIMM (Single Inline MemoryModule), DIMM (Dual Inline Memory Module), etc. of a memory board if needed.

[0003] However, since the dimension has become settled by specification, if SIMM and DIMM constitute a memory board using the memory IC by which packaging was carried out, since the dimension of the package of Memory IC itself is large, they can seldom increase memory space.

[0004]

[Problem(s) to be Solved by the Invention] In order to solve such a problem, as shown in drawing 9 , the memory module which increases memory space twice by mounting memory IC in piles up and down is proposed. The memory module of drawing 9 repeats the DRAM chip enclosed with TCP (Tape Carrier Package)101 of a super-thin shape on a memory module substrate at two steps of one side. Since the dimension of TCP hardly changes to the dimension of the bare chip cut down from the semi-conductor wafer, even if mounted in two steps in piles, it can fulfill the specification of SIMM or DIMM.

[0005] However, in order that the memory module shown in drawing 9 may pull out the leadframe 102 separately from TCP101 of the upper stage and a lower stage, respectively and may connect these leadframes 102 with a substrate altogether, mounting takes time and effort, and it is easy to generate defects, such as a short circuit of a leadframe 102, and an open circuit, and there is a possibility that a manufacturing cost may rise.

[0006] This invention is created in view of such a point, the purpose is easy to mount and it is to offer the semiconductor device which can improve packaging density.

[0007]

[Means for Solving the Problem] In order to solve the technical problem mentioned above, the semiconductor device of claim 1 is characterized by having mounted the 2nd bare chip in the top face of the 1st bare chip, and making it two-step structure. The pad on the 1st bare chip and the pad on the 2nd bare chip are connected through a bump. That is, flip chip mounting of the 2nd bare chip is carried out on the 1st bare chip. On the 1st bare chip, two or more pads also including the part of the input/output terminal of the 2nd bare chip are formed, and these pads and the pad on

a substrate are connected by the bonding wire. Therefore, it is not necessary to carry out direct continuation of the 2nd bare chip and substrate, and a wirebonding activity is simplified.

[0008] The semiconductor device of claim 2 forms the 1st pad train for carrying out flip chip mounting of the 2nd bare chip in the inner circumference side of the top face of the 1st bare chip, and forms the 2nd pad train for bonding wire connection in the periphery side. For this reason, a bonding wire can be attached in the 2nd pad train also after mounting the 2nd bare chip.

[0009] The semiconductor device of claim 3 consists of one bare chip, and a pad is formed in both sides of a bare chip. The pad of the inferior surface of tongue of a bare chip is used for a substrate in order to carry out flip chip mounting, and a pad on top is used in order to carry out COB mounting at a substrate. It is not necessary to make extremely narrow between the pads which adjoin in order to make [of a bare chip] connection with a substrate from both sides and, and since it is not two-step structure, thickness of a semiconductor device can be made thin.

[0010] The semiconductor device of claim 4 is characterized by having mounted the 2nd bare chip in the inferior surface of tongue of the 1st bare chip, and making it two-step structure. Flip chip mounting of the 2nd bare chip is carried out on a substrate, and the pad formed in the top face of the 1st bare chip is connected with the pad on a substrate through a bonding wire.

[0011] The semiconductor device of claim 5 carries out flip chip mounting of the 2nd bare chip on the inferior surface of tongue of the 1st bare chip. Two or more pads also including the part of the input/output terminal of the 2nd bare chip are formed in the top face of the 1st bare chip, and these pads and the pad on a substrate are connected by the bonding wire.

[0012] The semiconductor device of claim 6 is characterized by having mounted the 2nd bare chip in the inferior surface of tongue of the 1st bare chip, and making it two-step structure. Flip chip mounting of the 2nd bare chip is carried out on the inferior surface of tongue of the 1st bare chip, and the inferior surface of tongue of the 2nd bare chip is connected with a substrate by adhesives etc.

[0013] Since the semiconductor device of claim 7 uses one stage as a CPU chip and considers the stage of another side as a memory chip or a CPU circumference chip, it can accelerate an exchange of the signal during these chips, and can avoid the effect of the noise by leading about of a signal line.

[0014] Since the semiconductor device of claim 8 piles up two memory chips, it can raise the packaging density of a memory board twice.

[0015]

[Embodiment of the Invention] Hereafter, the semiconductor device which applied this invention is explained concretely, referring to a drawing.

[0016] [1st operation gestalt] The perspective view of the 1st operation gestalt of the

semiconductor device which drawing 1 requires for this invention, and drawing 2 are the sectional views of the A-A line of drawing 1 . As shown in these drawings, the semiconductor device of this operation gestalt has the structure which put the 1st and 2nd bare chips 1 and 2 cut down from the semi-conductor wafer on two steps. The 1st bare chip 1 is a CPU chip, and the 2nd bare chip 2 is a memory chip.

[0017] As shown in drawing 2 , two or more pads 3 are formed in the component forming face of the 1st bare chip 1, and two or more pads 4 are formed also in the component forming face of the 2nd bare chip 2 corresponding to these pads. A component forming face is turned down, namely, a face down is carried out, and flip chip mounting of the 2nd bare chip 2 is carried out on the component forming face of the 1st bare chip 1. About the detail of flip chip mounting, it mentions later.

[0018] Drawing 3 (a) and (b) are drawings having simplified and shown the structure of the component forming face of the 1st and 2nd bare chips 1 and 2, respectively. As shown in drawing 3 (a), two or more pads are formed in two trains by the side of inner circumference and a periphery at the component forming face of the 1st bare chip 1. It is prepared in order to connect the pad 3 by the side of inner circumference with the 2nd bare chip 2, and the pad 5 by the side of a periphery is formed in order to carry out COB mounting at a printed wired board 6. The pad 5 by the side of a periphery is formed corresponding to each of the input/output terminal of the 1st and 2nd bare chips 1 and 2, and the pad corresponding to the input/output terminal of the 2nd bare chip 2 is connected with the pad 3 by the side of inner circumference through the circuit pattern 10 on the 1st bare chip 1 among the pads 5 by the side of a periphery.

[0019] On the other hand, the pad 4 of the same number is formed in the component forming face of the 2nd bare chip 2 at the pad 3 and this spacing by the side of the inner circumference of the 1st bare chip 1. The pad 3 of the 1st bare chip 1 and the pad 4 of the 2nd bare chip 2 are connected through the bumps 7, such as a solder ball metallurgy ball, as shown in drawing 2 . By performing such flip chip mounting, as for the pad 4 of the 2nd bare chip 2, an electric flow with the pad 5 by the side of the periphery of the 1st bare chip 1 is secured through a bump 7, the pad 3 by the side of the inner circumference of the 1st bare chip 1, and a circuit pattern 10.

[0020] Drawing 4 is drawing showing the production process of the semiconductor device of this operation gestalt. First, a bump 7 is attached in the pad 4 on the 2nd bare chip 2 cut down from the semi-conductor wafer as shown in drawing 4 (a). Next, as shown in drawing 4 (b), the component forming face of the 2nd bare chip 2 is turned down, and it joins to the 1st bare chip 1. Next, after positioning the 1st bare chip 1 on a printed wired board 6, as shown in drawing 1 , the pad 5 by the side of a periphery and the pad 8 on a printed wired board 6 are connected by the bonding wire 9. Next, in order to protect the body of a chip, and a bonding wire 9, the whole front face of the semiconductor device mounted on the printed wired board 6 is covered by resin.

wired board 6 through the pad 14 by the side of the top face of the 3rd bare chip 11 among the input/output terminals which the 4th bare chip 12 has, and the remaining input/output terminals are connected with the printed wired board 6 through the pad 13 and bump 15 by the side of the inferior surface of tongue of the 4th bare chip 12.

[0027] Thus, since the semiconductor device of the 2nd operation gestalt pulls out a bonding wire 9 only from the bare chip 11 of the upper stage, it can make the height of a bonding wire 9 regularity mostly. Moreover, since it connects with a printed wired board 6 through the bare chip 11 of the upper stage and only the remaining input/output terminals are connected with a printed wired board 6 through a bump 15, a part of input/output terminal which the bare chip 12 of a lower stage has can reduce the number of bumps 15, and even if there are many input/output terminals, it can mount it reasonable.

[0028] If the pad corresponding to all the input/output terminals that the 4th bare chip 12 has is prepared in the top face of the 3rd bare chip 11, it will become unnecessary in addition, to carry out flip chip mounting of the 4th bare chip 12 on a printed wired board 6. For this reason, as shown in drawing 7 (a), while the 4th bare chip 12 can be directly pasted up on a printed wired board 6 with adhesives etc. and a mounting activity becomes easy, the thickness of a semiconductor device also becomes thin.

[0029] If the pad corresponding to all the input/output terminals that the 4th bare chip 12 has is prepared in the inferior surface of tongue of the 4th bare chip 12, it will become unnecessary on the contrary, to carry out flip chip mounting of the 4th bare chip 12 at the 3rd bare chip 11. For this reason, as shown in drawing 7 (b), both chips become possible [pasting up directly with adhesives etc.].

[0030] By the way, although the 1st and 2nd operation gestalten mentioned above explained the example which piles up a CPU chip and a memory chip up and down, as a class of bare chip piled up up and down, a CPU chip and various bare chips other than a memory chip, such as a CPU circumference chip and a graphic chip, can be considered. For example, if the 1st and 2nd bare chips 1 and 2 are made [both] into a memory chip, the memory space per unit component-side product can be increased twice. Moreover, if a CPU circumference chip is used as a bare chip of another side, using a CPU chip as one bare chip, since a signal can be exchanged at a high speed among these chips, the clock rate of CPU can be made more into a high speed.

[0031] Although the operation gestalt mentioned above showed the example which piled up two kinds of bare chips up and down, as shown in drawing 8 , the pad for flip chip mounting is formed, the pad for the object for COB mounting, i.e., bonding wire connection, may be formed in a top-face side, and connection with a substrate may be made [of a bare chip] to the one inferior-surface-of-tongue side of a bare chip from both sides.

[0032] If mounting like drawing 8 is performed, even if it is the LSI bare chip of high

[0021] Thus, since the semiconductor device of this operation gestalt has the structure which piled up two kinds of bare chips 1 and 2 up and down and carries out flip chip mounting of the bare chip 2 of an upper case on the bare chip 1 of the lower berth, it can make thickness of the whole semiconductor device thin. Therefore, it can mount in severe SO-DIMM, SIMM, etc. of clearance reasonable.

[0022] Moreover, since the pad 5 for external connection was formed only in the bare chip 1 of a lower stage, it becomes easy to give the wirebonding activity at the time of carrying out COB mounting to a printed wired board 6. Since it is not necessary to pull out a bonding wire 9 from the bare chip 2 of the upper stage especially, defect incidence rates, such as a short circuit of a bonding wire 9 and an open circuit, can be stopped low. Moreover, since the bare chip 2 of the upper stage of what needs to change the structure of the bare chip 1 of a lower stage can use the conventional chip as it is, it does not become a large design change. For example, when the 1st bare chip 1 is used as a CPU chip and the 2nd bare chip 2 is made into a memory chip, about a memory chip, elegance can be used as it is conventionally that what is necessary is just to carry out the partial change only of the component structure of a CPU chip.

[0023] Moreover, the pad 4 of the bare chip 2 of the upper stage is connected with the pad 5 by the side of the periphery of the bare chip 1 of a lower stage through the bump 7 or the circuit pattern 10, and since the bonding wire 9 is not used for connection, even if it prepares the pad corresponding to the input/output terminal of the bare chip 2 of the upper stage in a lower stage, the amount of signal delay does not become a problem, and it is hardly influenced by the noise.

[0024] [2nd operation gestalt] As for the 1st operation gestalt, the 2nd operation gestalt explained below pulls out a bonding wire from the upper case side of the semiconductor device of two-step structure conversely.

[0025] Drawing 5 is the perspective view of the semiconductor device of the 2nd operation gestalt, and drawing 6 is the B-B line sectional view of drawing 5 . As shown in these drawings, the semiconductor device of the 2nd operation gestalt has the structure which piled up the 3rd and 4th bare chips 11 and 12 up and down, and the pad 13 formed in the inferior-surface-of-tongue side of the 3rd bare chip 11 and the pad 14 formed in the top-face side of the 4th bare chip are connected through the bump 15. Two or more pads 16 are formed in the top-face side of the 3rd bare chip 11, and these pads 16 and the pad 8 on a printed wired board 6 are connected by the bonding wire 9. Moreover, two or more pads 17 are formed in the inferior-surface-of-tongue side of the 4th bare chip 12, and flip chip mounting of these pads 17 is carried out on a printed wired board 6 through a bump 15.

[0026] The pad 14 by the side of the top face of the 4th bare chip 12 has flowed electrically through a bump 15, the pad 13 by the side of the inferior surface of tongue of the 3rd bare chip 11, and a non-illustrated circuit pattern with the pad 16 by the side of the top face of the 3rd bare chip 11. That is, a part is connected with a printed

accumulation with many input/output terminals, it can mount without making between pads extremely narrow.

[0033]

[Effect of the Invention] As explained to the detail above, according to this invention, it can write in the two-step structure which piled up the 1st and 2nd bare chips up and down, a component-side product can be made into abbreviation one half, and high density assembly becomes possible. Moreover, since a bare chip is piled up up and down, thickness of a semiconductor device can be made thin and can be mounted in the severe SO-DIMM substrate of clearance etc. reasonable.

[0034] Moreover, in order to form the pad for external connection only in one of bare chips, it becomes easy to do the wirebonding activity in the case of performing COB mounting, and the incidence rate of defects, such as a short circuit of a bonding wire and an open circuit, also becomes low.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the perspective view of the 1st operation gestalt of the semiconductor device concerning this invention.

[Drawing 2] It is the A-A line sectional view of drawing 1 .

[Drawing 3] They are drawing in which (a) simplified and showed the structure of the component forming face of the 1st bare chip, and drawing which (b) simplified the structure of the component forming face of the 2nd bare chip, and was shown.

[Drawing 4] It is drawing showing the production process of the semiconductor device of this operation gestalt.

[Drawing 5] It is the perspective view of the 2nd operation gestalt of the semiconductor device concerning this invention.

[Drawing 6] It is the B-B line sectional view of drawing 5 .

[Drawing 7] The example in which (a) pasted up the 4th bare chip directly on the printed wired board, and (b) are drawings showing the example which pasted up the 3rd bare chip and 4th bare chip directly.

[Drawing 8] It is drawing which constituted the semiconductor device from one bare chip.

[Drawing 9] It is drawing showing the conventional example of the memory module which made memory IC the two-step pile.

[Description of Notations]

1 1st Bare Chip

2 2nd Bare Chip

3– 5 and 8 Pad

6 Printed Wired Board

7 Bump

9 Bonding Wire

10 Circuit Pattern